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10/602,730	06/25/2003	Joo-Yul Lee	6161.0063.AA	8848

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,730	LEE, JOO-YUL	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 28 November 2005. Claims 1-11 are pending.

Response to Arguments

2. Applicant's arguments filed 28 November 2005 have been fully considered but they are not persuasive.

The applicant argues that the amended independent claims 1, 5 and 11 are not anticipated by Roh, since Roh has a separate main path (Yp) and falling ramp (Yfr) switches and that the main path switch as claimed by the applicant is a single switch having a Yp component linked to a Yfr. However, the examiner interprets that the switches Yp and Yfr function together as the main path switch which is claimed, wherein the main path switch would include "a falling ramp switch integrated therein" as recited by claim 5 and would function "for generating a falling ramp waveform which is a portion of a reset waveform," as recited by claims 1 and 11.

Claim Objections

3. Claim 7 is objected to because of the following informalities:

Claim 7 currently reads: "The method of claim 5, wherein charging, to a third voltage, a capacitor having a first end selectively coupled to a first voltage and a second voltage, comprises *timing on a first switch coupled to the first voltage is turned on to supply the first voltage to the first end of the capacitor.*" The claim fails to make sense as stated.

The examiner suggests changing the claim to read: "The method of claim 5, wherein charging, to a third voltage, a capacitor having a first end selectively coupled to a first voltage and a second voltage, comprises *turning on a first switch coupled to the first voltage to supply the first voltage to the first end of the capacitor.*"

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Roh (US 6,617,802).

Regarding claim 1, Roh discloses a device for driving a PDP (plasma display panel) for arranging a plurality of scan electrodes and sustain electrodes to be crossed with the scan electrodes and the sustain electrodes (Figure 5, item 300 represents the plurality of scan electrodes, sustain electrodes, and the address electrodes being crossed with the scan and sustain electrodes), the device comprising:

a first switch and a second switch coupled in series between a first voltage and a second voltage (Figure 5 shows a first switch SY1 and second switch Sy2 coupled in series between a first voltage Vs and a second voltage ground);

a capacitor coupled between a contact point of the first switch and the second switch and a third voltage (Figure 5 shows a capacitor Cset coupled between SY1 and Sy2 and Vset, where Vset is the third voltage);

a rising ramp switch for forming a constant current is coupled to the third voltage at a first end of the rising ramp switch (Figure 5 shows switch Yrr as being a rising ramp switch that is coupled to Vset); and

a main path switch (Figure 5, Yp and Yfr function together as a main path switch) coupled between the contact point of the first and second switches and second end of the rising ramp switch, for forming a constant current and for generating a falling ramp waveform which is a portion of a reset waveform (Figure 5 shows a main path switch, Yp and Yfr, as being coupled to the second

end of Yrr and the contact point between SY1 and Sy2 where Yp is for forming constant current and Yfr generates a falling ramp waveform).

Regarding claim 2, Roh discloses the device of claim 1, wherein the first voltage is a sustain voltage, the second voltage is a ground voltage, and the third voltage is a voltage that is high enough that a sum of the third voltage and the first voltage may uniformly redistribute wall charges of respective cells of the PDP (In Figure 5, the examiner interprets the first voltage as being Vs and the sustain voltage, the second voltage to be the ground connection to Sy2, and it would be inherently known to have the third voltage high enough such that a sum of the third and first voltage would be high enough to uniformly redistribute wall charges of respective cells of the PDP).

Regarding claim 3, Roh discloses the device of claim 1, wherein the first and second switches, the rising ramp switch, and the main path switch are MOS transistors wherein each MOS transistor has a body diode (Column 6, lines 52-54 it states: "The apparatus of claim 4, wherein the diode is a body diode, which is embedded in the respective MOSFET switch.").

Regarding claim 4, Roh discloses the device of claim 1, wherein each of the rising ramp switch and the main path switch includes a MOS transistor having a gate and a drain between which a capacitor is coupled (having a capacitor coupled between the gate and drain of a MOS transistor is inherent in the art).

Regarding claim 5, Roh discloses a method for driving a PDP (plasma display panel) for arranging a plurality of scan electrodes and sustain electrodes in parallel for each display line, and arranging a plurality of address electrodes to be crossed with the scan electrodes and the sustain electrodes (Figure 5 shows a method for driving a PDP, items 100, 200 and 500, having item 300 which includes the scan, sustain and address electrodes), the method comprising:

charging, to a third voltage, a capacitor having a first end selectively coupled to a first voltage and a second voltage (Figure 5 shows Vset, a third voltage, which can charge capacitor Cset to that voltage, having Cset's first end selectively coupled to a first voltage, Vs and a second voltage being ground);

supplying the first voltage to the first end of the capacitor (In Figure 5, Vs, the first voltage, can be supplied to the first end of Cset), and

turning on a rising ramp switch for supplying a constant current to the scan electrode to make the potential of the scan electrode rise to the third voltage from the first voltage in a ramp waveform (In Figure 5, Yrr can be turned on to a supply constant current to the scan electrode),

the rising rap switch being coupled between a second end of the capacitor and the scan electrode (Figure 5 shows Yrr, the rising ramp switch, to be coupled between capacitor Cset and the scan electrode in item 300);

turning off the rising ramp switch (In Figure 5, Yrr can be turned off), and

supplying the second voltage to the first end of the capacitor to control the potential of the scan electrode to a fourth voltage (In Figure 5, the ground

voltage, being the second voltage, can be applied to the first end of Cset to control the potential of the scan electrode to a fourth voltage); and

turning on a main path switch for supplying the constant current to the scan electrode to make the potential of the scan electrode gradually fall (In Figure 5, Yp and Yfr which work together as the main path switch, can be turned on to supply constant current to the scan electrode to make the potential gradually fall),

the main path switch being coupled between the second voltage and the scan electrode (Figure 5 shows Yp and Yfr, the main path switch, coupled between ground, the second voltage, and the scan electrode, item 300),

wherein the main path switch includes a falling ramp switch integrated therein (Figure 5, the main path switch, Yp and Yfr, has a falling ramp switch, Yfr, integrated therein.).

Regarding claim 6, Roh discloses the method of claim 5, wherein the first voltage is a sustain voltage, the second voltage is a ground voltage, the third voltage is a voltage high enough that the sum of the third voltage and the first voltage may uniformly redistribute wall charges of respective cells of the PDP, and the fourth voltage is the third voltage (Figure 5 shows Vs, being the first voltage and the sustain voltage, the second voltage being ground, it would be inherently known to have the third voltage high enough such that a sum of the third and first voltage would be high enough to uniformly redistribute wall charges

of respective cells of the PDP, and since the second voltage is ground, the fourth voltage would have to be equal to that of the third).

Regarding claim 7, Roh discloses the method of claim 5, wherein charging, to a third voltage, a capacitor having a first end selectively coupled to a first voltage and a second voltage (Figure 5 shows a capacitor Cset coupled between Vs and ground and Vset, where Cset can be charged to Vset), comprises turning on a first switch coupled to the first voltage to supply the first voltage to the first end of the capacitor (Figure 5 shows a switch SY1 coupled to the first voltage Vs and can be turned on to supply Vs to the first end of Cset).

Regarding claim 8, Roh discloses the method of claim 5, wherein

supplying the first voltage to the first end of the capacitor (In Figure 5, Vs, the first voltage, can be supplied to the first end of Cset), and

turning on a rising ramp switch for supplying a constant current to the scan electrode to make the potential of the scan electrode rise to the third voltage from the first voltage in a ramp waveform (In Figure 5, Yrr can be turned on to a supply constant current to the scan electrode) comprises

supplying the first voltage to the first end of the capacitor by having current flow through a charge and discharge unit coupled to a contact point of a first switch and a second switch coupled in series between the first voltage and the second voltage (In Figure 5, item 500 shows a charge and discharge unit that is coupled to the switches SY1, the first switch, and Sy2, the second switch. This

item 500 could have current pass through it to supply voltage to the first end of the capacitor Cset from Vs, the first voltage).

Regarding claim 9, Roh discloses the method of claim 5, wherein

turning off the rising ramp switch (In Figure 5, Yrr can be turned off), and

supplying the second voltage to the first end of the capacitor to control the potential of the scan electrode to a fourth voltage (In Figure 5, the ground voltage, being the second voltage, can be applied to the first end of Cset to control the potential of the scan electrode to a fourth voltage) comprises

turning on a second switch coupled to the second voltage to supply the second voltage to the first end of the capacitor (In Figure 5, Sy2, the second switch, could be turned on which would supply the second voltage, ground, to the first end of the capacitor).

Regarding claim 10, Roh discloses the method of claim 5, wherein

turning off the rising ramp switch (In Figure 5, Yrr can be turned off), and

supplying the second voltage to the first end of the capacitor to control the potential of the scan electrode to a fourth voltage (In Figure 5, the ground voltage, being the second voltage, can be applied to the first end of Cset to control the potential of the scan electrode to a fourth voltage) comprises

supplying the second voltage to the first end of the capacitor by having current flow through a charge and discharge unit coupled to a contact point of a first switch and a second switch and a second switch coupled between the first

voltage and the second voltage (In Figure 5, item 500 shows a charge and discharge unit that is coupled to the switches SY1, the first switch, and Sy2, the second switch. This item 500 could have current pass through it to supply voltage to the first end of the capacitor Cset from the second voltage, ground).

Regarding claim 11, Roh discloses a plasma display panel (PDP) comprising: a first substrate and a second substrate (It is inherently known that a PDP would comprise of a first and second substrate);

a plurality of scan electrodes and sustain electrodes arranged in pairs (Shown in Figure 5, item 300);

a plurality of data electrodes arranged to be crossed with the scan electrodes and the sustain electrodes (Shown in Figure 5, item 300);

a first switch and a second switch coupled in series between a first voltage and a second voltage (Figure 5 shows a first switch SY1 and second switch Sy2 coupled in series between a first voltage Vs and a second voltage ground);

a capacitor coupled between a contact point of the first and second switches and a third voltage (Figure 5 shows a capacitor Cset coupled between SY1 and Sy2 and Vset, where Vset is the third voltage);

a rising ramp switch coupled to the third voltage, for forming a constant current (Figure 5 shows switch Yrr as being a rising ramp switch that is coupled to Vset); and

a main path switch (Figure 5, Yp and Yfr function together as a main path switch) coupled between the contact point of the first and second switches and

another end of the rising ramp switch, for forming a constant current and for generating a falling ramp waveform which is a portion of a reset waveform (Figure 5 shows switches Yp and Yfr as being coupled to the second end of Yrr and the contact point between SY1 and Sy2 where Yp is for forming constant current and Yfr generates a falling ramp waveform).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER

7 December 2005